Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

What is claimed is:

1-14. (Cancelled).

15. (Original) A platform comprising:

a memory device to store a system Basic Input/Output System (BIOS); and

a plurality of processor substrates in communication with the memory device, the plurality of processor substrates including

a first processor substrate including a first plurality of components and a first storage device to contain a first initialization BIOS to initialize the first plurality of components in response to hot-plug addition of the first processor substrate to the platform, and

a second processor substrate including a second plurality of components and a second storage device to contain a second initialization BIOS to initialize the second plurality of components in response to hot-plug addition of the second processor substrate to the platform.

16. (Currently Amended) The platform of claim ~~12~~15, wherein the first plurality of components of the first processor substrate include a processor cluster and a memory cluster.

17. (Currently Amended) The platform of claim ~~13~~16, wherein the first plurality of components of the first processor substrate further include a scalability node controller coupled to the processor cluster and the memory cluster.

18. (Currently Amended) The platform of claim ~~14~~17, wherein the scalability node controller of the first plurality of components is coupled to local memory of the memory cluster

through a plurality of communication sub-links supporting a total data throughput of at least one Gigabyte per second.

19. (Currently Amended) The platform of claim ~~14~~17, wherein the scalability node controller of the first plurality of components includes a plurality of scalability port interfaces coupled to a first connector of the first processor substrate.

20. (Currently Amended) The platform of claim ~~16~~19, wherein the second plurality of components of the second processor substrate further include a secondary scalability node controller including a plurality of scalability port interfaces coupled to a second connector of the second processor substrate.

21. (Currently Amended) The platform of claim ~~17~~20 further comprising:

an interconnect substrate including a third connector, a fourth connector and a fifth connector, the third connector adapted to mate with the first connector of the first processor substrate and coupled to the fifth connector via a first link and a second link, the fourth connector adapted to mate with the second connector of the second processor substrate and coupled to the fifth connector via a third link and a fourth link.

22. (Currently Amended) The platform of claim ~~18~~21 further comprising:

an input/output (I/O) substrate including a sixth connector coupled to the fifth connector, the I/O substrate further includes (1) a first scalability port switch coupled to the first link and the third link, (2) a second scalability port switch coupled to the second link and the fourth link, (3) a first Server Input/Output Hub coupled to the first and second scalability port switches, and (4) a second Server Input/Output Hub coupled to the first and second scalability port switches.

23. (Currently Amended) The platform of claim ~~19~~22, wherein the first initialization BIOS contained in the first storage device, when executed, also establishes a communication path between the scalability node controller and at least one of the first scalability port switch and the second scalability port switch.

24. (Currently Amended) The platform of claim ~~19~~22, wherein the second initialization BIOS contained in the second storage device, when executed, also establishes a communication path between the secondary scalability node controller and at least one of the first scalability port switch and the second scalability port switch.

25. (Currently Amended) The platform of claim ~~13~~16, wherein the first initialization BIOS contained in the first storage device elects a processor from a plurality of processors associated with the processor cluster to act as a node boot strap processor for the first processor substrate.

26. (Currently Amended) The platform of claim ~~12~~15, wherein the second initialization BIOS contained in the second storage device elects a processor from a plurality of processors implemented on the second processor substrate to act as a node boot strap processor for the second processor substrate.

27. (Currently Amended) The platform of claim ~~12~~15, wherein the first initialization BIOS contained in the first storage device initializing the first plurality of components prior to notification of an operating system running on the platform of the initialized hot-plugged first processor substrate.

28. (Original) A platform comprising:

a first processor substrate including a first plurality of components and a first storage device to contain a first code segment of Basic Input/Output System (BIOS) that, when executed, initializing the first plurality of components in response to hot-plug addition of the first processor substrate to the platform; and

a second processor substrate including a second plurality of components and a second storage device to contain a second code segment of BIOS that, when executed, initializing the second plurality of components in response to hot-plug addition of the second processor substrate to the platform.

29. (Currently Amended) The platform of claim ~~25~~28 further comprising:

an interconnect substrate including a first connector, a second connector and a third connector, the first connector being adapted to mate with a connector of the first processor substrate that is coupled to a plurality of scalability port interfaces of a first scalability node controller of the first plurality of components, the second connector being adapted to mate with a connector of the second processor substrate that is coupled to a plurality of scalability port interfaces of a second scalability node controller of the second plurality of components, and a third connector coupled to both the first connector via a first link and a second link and the second connector via a third link and a fourth link.

30. (Currently Amended) The platform of claim ~~26~~ 29 further comprising:

an input/output (I/O) substrate including a fourth connector coupled to the third connector, the I/O substrate further includes (1) a first scalability port switch coupled to the first link and the third link, and (2) a second scalability port switch coupled to the second link and the fourth link.

31. (Currently Amended) The platform of claim ~~27~~30, wherein the first code segment of BIOS, when executed, also establishes a communication path between the first scalability node controller and at least one of the first scalability port switch and the second scalability port switch.

32. (Currently Amended) The platform of claim ~~28~~31, wherein the second code segment of BIOS, when executed, also establishes a communication path between the second scalability node controller and at least one of the first scalability port switch and the second scalability port switch.

33. (Currently Amended) The platform of claim ~~25~~28, wherein the first code segment of BIOS initializing the first plurality of components prior to notification of an operating system running on the platform of the first plurality of components upon hot-plug addition of the first processor substrate.

34. (Original) A platform comprising:

an operating system;

an input/output (I/O) substrate including (i) a first scalability port switch, (ii) a second scalability port switch, (iii) a first server I/O hub and (iv) a second server I/O hub;

a first processor substrate including a first plurality of components in communication with the first and second scalability port switches; and

a second processor substrate including a second plurality of components and circuitry to support dynamic partitioning of the platform by signaling the operating system of a hot-plug removal of the second server I/O hub and the second plurality of components to cause the operating system to configure the first scalability port switch and the second scalability port switch so as to partition the platform into a first platform including the first plurality of components and the first server I/O hub and a second platform including the second plurality of components and the second server I/O hub.

35. (Original) The platform of claim 34, wherein the second platform is able to run an updated software application independent of and without interrupting operations of the first platform.

36. (Original) The platform of claim 35, wherein the updated software application is an updated operating system.

37. (Original) A method comprising:

providing a multi-node platform under control of an operating system, the multi-node platform including a first processor substrate and a second processor substrate in communication with an input/output (I/O) substrate; and

implementing a portion of a Basic Input/Output Subsystem (BIOS) on the first processor substrate to initialize components on the first processor substrate in response to hot-plug addition of the first processor substrate before joining the running operating system.

38. (Original) The method of claim 37 further comprising:

implementing a portion of the BIOS on the second processor substrate to initialize components on the second processor substrate in response to hot-plug addition of the second processor substrate before joining the running operating system.

39. (Original) The method of claim 37, wherein the components on the first processor substrate include at least two processors.